IN THE SPECIFICATION

Please replace the paragraph at page 2, lines 8-14, with the following rewritten paragraph:

Referring to FIGS. 19A and 19B, "parallel" refers to a situation where the spinning directions of the paired magnetic layers are identical, whereas "opposite parallel" refers to a situation where the spinning directions of the paired magnetic layers are opposite relative to each other (arrows ~~indicate~~ indicated show spinning directions).

Please replace the paragraph at page 2, lines 22-26, with the following rewritten paragraph:

The tunnel resistance of the insulating layer (tunnel barrier layer) sandwiched ~~by~~ between the paired magnetic layers is minimized when the spinning directions of the two magnetic layers are in parallel as shown in FIG. 19A. This state may be "1" state.

Please replace the paragraph at page 11, lines 19-22, with the following rewritten paragraph:

The present invention will be described with reference to the accompanying drawings. The components identical or similar to one another are denoted ~~at~~ with the same reference symbols in the drawings.

Please replace the paragraph at page 14, lines 11-22, with the following rewritten paragraph:

The plurality of read word lines RWL0, ..., RWL7 and the plurality of write word lines WWL0, ..., WWL7 intersect the bit lines BL00, ..., BL3N typically in memory cell array 7. The read word lines RWL0, ..., RWL7 are connected at an end thereof to the read

word line driver circuit of read word line driver circuit/write word line driver circuit (RWL. DRV./WWL. DRV.) 8. The ~~read~~ write word lines WWL0, ..., WWL7 are connected at an end thereof to the write word line driver circuit of read word line driver circuit/write word line driver circuit 8 and at the other end to write word line sinker circuit (WWL. SNK.) 9.

Please replace the paragraph at page 15, lines 13-17, with the following rewritten paragraph:

For instance, as shown in an equivalent circuit diagram of FIG. 2 each memory cell may be adapted to use a MOSFET as a switching element. The MOSFET that operates as a switching element may be replaced by a diode.

Please replace the paragraph beginning at page 17, line 24, through page 18, line 1, with the following rewritten paragraph:

As shown in FIGS. 5A through 5D, this first example of a memory cell that ~~include~~ includes a magneto-resistive element is a 1-magnetoresistive element/1-transistor type memory cell having a magneto-resistive element 12 and a cell transistor 13.

Please replace the paragraph at page 23, lines 12-15, with the following rewritten paragraph:

For example, a cell realized by using a diode in place of a transistor as a switching element as shown in FIG. 8 or a cross point type cell having no switching element as shown in FIG. 9 may be used.

Please replace the paragraph at page 23, lines 22-25, with the following rewritten paragraph:

TMR elements can be used for the magneto-resistive effect elements 3 described above for the first through third embodiments. Now, several examples of TMR ~~element~~ elements will be described below.

Please replace the paragraph at page 33, lines 15-21, with the following rewritten paragraph:

In the present example, two types of memories of the magnetic random access memory 170 and EEPROM 180 are used as a memory to ~~hole~~ hold the line code program. However, the EEPROM 180 can be replaced by a magnetic random access memory. That is, instead of using two types of memories, only the magnetic random access memory can be used.